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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,017	01/28/2004	Toshio Miyazawa	6453P034	4732

8791 7590 08/20/2008

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EXAMINER	
RASHID, DAVID	

ART UNIT	PAPER NUMBER
2624	

MAIL DATE	DELIVERY MODE
08/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,017	MIYAZAWA ET AL.	
	Examiner	Art Unit	
	DAVID P. RASHID	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Amendments

[1] This office action is responsive to the Amendment and Response to Office Action received on June 27, 2008. Claims 1-17 remain pending.

Response to Arguments

[2] Applicant's Remarks filed July 26, 2008 with respect to claims 1-17 have been respectfully and fully considered, but are not found persuasive.

Summary of First Remark regarding claims 1, 2, 5, 9, 11, and 13

> Applicant respectfully submits that, although the Examiner is entitled to the broadest reasonable interpretation of the claim, the interpretation must be consistent with the specification. M.P.E.P. § 2111, citing *Phillips v A WH Corp.,* 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005). As such, the Examiner should interpret the claim terms of "first-level storing unit," and "second-level storing units," in light of the specification as it would be interpreted by one of ordinary skill in the art. M.P.E.P. § 2111, citing *In re Am. Acad. of Sci. Tech. Ctr.,* 367 F.3d 1359, 1364. In the present case, the Office action appears to equate memory address as a storage unit, and interprets the memory address responsible for storing the compressed codes of the first hierarchical layer as being separate from the memory addresses responsible for storing the compressed codes of the second hierarchical layer.
>
> The Applicant's specification, however, describes the storing units as separate storing units, not separate memory addresses of the same storing unit. For example, the Applicant's specification described that the storage unit 46, as illustrated in Figure 9, as being formed by a hard disk drive (HDD) or the like, which stores various programs and various data. Applicant's Specification, page 25, paragraph 77, lines 3-4. The Applicant's specification also describes in the context of the server computer of Figure 10 that the HDD 15, which stores the compressed codes, is part of the secondary storage unit 16, as contrasted with the primary storage unit 14, which includes a RAM 13 and a ROM 14. Also, with respect to Figure 11, Applicant's specification describes three different level data storage units, the first having the HDD 15 of the server computer that stores the highest hierarchical layer, the second having the storage unit 46 of the client computer 4 that stores the second highest hierarchical layer, and a third storage unit 46 of another client computer that stores the lowest hierarchical layer. Thus the first-level and second level storing units are described as being separate secondary storage units, including HDD or the like, to store the compressed codes for the particular level, not separate memory addresses. Here, the Office action, in an effort to read the claims on the cited reference, has incorrectly interpreted storing units to mean memory addresses, because those memory addresses are physically separate from one another, even if those memory addresses reside in the same storage unit. This interpretation is not made in a manner that is consistent with the specification as it would be interpreted by one of ordinary skill in the art, and as such, is an improper interpretation of the claimed terms.

(Remarks at 11-12; *emphasis added.*)

Examiner's Response

However, restricting the "first-level storing unit" and "second-level storing unit" (Claim 1, Jun. 27, 2008) "as separate storing units, not separate memory addresses of the same storing unit" (Remarks at 11-12) is unpersuasive for several reasons.

M.P.E.P. § 2111 titled "Claim Interpretation; Broadest Reasonable Interpretation" cites, in relevant part:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's *en banc* decision in Phillips v. AWH Corp., 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard:
>
> The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." In re Am. Acad. of Sci. Tech. Ctr., 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004)." Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

M.P.E.P. § 2111.

Furthermore, M.P.E.P. § 2111.01 (IV) cites, in relevant part:

> An applicant is entitled to be his or her own lexicographer and may rebut the presumption that claim terms are to be given their ordinary and customary meaning by clearly setting forth a definition of the term that is different from its ordinary and customary meaning(s). *See* In re Paulsen, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (inventor may define specific terms used to describe invention, but must do so "with reasonable clarity, deliberateness, and precision" and, if done, must "set out his uncommon definition in some manner within the patent disclosure' so as to give one of ordinary skill in the art notice of the change" in meaning) (*quoting* Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 1992)).

M.P.E.P. § 2111.01 (IV).

The Examiner cannot find any definite language in the original disclosure that restricts a "storing unit" to something other than memory addresses (see below arguing that all electronic storage units must be composed of memory addresses). A "storing unit" would be interpreted by one of ordinary skill in the art as a "unit" capable of "storing". A "storing unit" under this simple

interpretation could be DRAM, SRAM, ROM, Williams tube, magnetic core memory, a piece of paper, etc. A memory address "is an identifier for a memory location, at which a computer program or a hardware device can store a piece of data for later retrieval." *See* http://en.wikipedia.org/wiki/Memory_address.

A "storing unit" could be read as broad as **a piece of paper** with information written on it, which the Examiner believes a true "broadest reasonable interpretation"; however, not one "consistent with the specification". *See* M.P.E.P. § 2111. A piece of paper is not consistent with the specification because the specification is disclosing electronic matter as related on a computer. Furthermore, **a chair** (though a broad interpretation) would be neither a reasonable interpretation of a storing unit nor one that is consistent with the specification.

However, **a memory address** is the basis of all electronic memory (a most fundamental unit of memory) that is in fact "consistent with the specification" as all of the storage units in the original disclosure must be comprised of memory addresses. There is not a memory equivalent of "storing unit" with that disclosed in the original disclosure that would not be comprised of memory addresses. In addition, the original disclosure even positively supports memory addresses when citing "hard disk drive (HDD) or the like" (*emphasis added*). An HDD is already composed of memory addresses, and the use of "or the like" supports that if not the HDD itself "as a whole", then a memory address would be an equivalent thereof.

In summary, the Examiner should be allowed to read memory addresses (a broad reasonable interpretation) as the broadly amended storage units consistent with the original disclosure, because memory addresses are "consistent with the specification" that is disclosing electronic hardware. The Examiner should not be restricted to interpreting a "storing unit" to

include matter that is not memory addresses, "hard disk drive (HDD)" and not "hard disk drive (HDD) or the like" (*emphasis added*), etc.

Summary of Second Remark regarding claims 1, 2, 5, 9, 11, and 13

> In addition, Applicant respectfully submits that nothing in Skodras expressly discloses how the compressed bit stream are stored, nonetheless, that the compressed bit streams are separately stored at particular memory addresses. Skodras only discloses that during the encoding process, the lengths and the distortions are computed and temporarily stored with the compressed bit stream itself, suggesting that the compressed bit streams are stored, but there is nothing in Skodras that discloses that a first set of memory addresses are responsible for storing the tiles, and that a second set of certain memory addresses that are physically separate from the first set for storing the precinct. Without such specificity, Skodras fails to disclose that the certain memory addresses are responsible for storing the first hierarchical layer, and that other memory addresses are responsible for storing the second hierarchical layer, as purported by the Office action. As such, Skodras fails to disclose all the limitations of the claim.

(Remarks at 12-13.)

Examiner's Response

However, the basic fact that *Skodras et al.* discloses (i) storing the JPEG 2000 hierarchically compressed and coded image data on memory; and (ii) that memory is composed of memory addresses is sufficient by reason of inherency. *See* M.P.E.P. § 2112 (citing that "express, implicit, and inherent disclosures of a prior art reference may be relied upon in the rejection of claims under 35 U.S.C. 102 or 103").

§ 2112 (III) (*emphasis added*) reads that "[w]here applicant claims a composition in terms of a function, property or characteristic and the composition of the prior art is the same as that of the claim but the function is not explicitly disclosed by the reference, the examiner may make a rejection under both 35 U.S.C. 102 and 103, expressed as a 102/103 rejection." Most importantly, "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent

characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990).

The Examiner provides the fact and technical reasoning that since (i) "storing units" are comprised and equivalent to memory addresses (*see* above argument); and (ii) the compressed codes of each hierarchical layer are being stored on said memory composed of memory addresses (*Skodras et al.* at fig. 2, "[c]ode [s]tream" in fig. 11) must be equivalent to a distributively storing unit that comprises

a first-level storing unit to store the compressed codes of the first hierarchical layer (it is inherent that there must exist memory addresses in the "[c]ode [s]tream" (*Skodras et al.* at fig. 11) that store the first hierarchical layer, that set of memory addresses being the "first-level storing unit")

a second-level storing unit to "separately" store the compressed codes of the second hierarchical layer (it is inherent that there must exist memory addresses in the "[c]ode [s]tream" (*Skodras et al.* at fig. 11) that store the second hierarchical layer, that set of memory addresses being the "second-level storing unit")

wherein the second-level storing unit is physically separate from the first-level storing unit (each memory address is physically separate from the others, thus it is inherent that the second-level storing unit is physically separate from the first-level storing unit).

The Examiner believes it is not required to show every memory address for which each bit is being sent in relation to which hierarchical layer it came from when the broad use of "storing unit" is being claimed (see above argument). Disclosing a code stream holding the separate hierarchical layers is sufficient, and the Examiner believes "a basis in fact and/or

technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art" has been shown with the argument given. *Ex parte Levy* at 1464. By reason of inherency, the "[c]ode [s]tream" of fig. 11 is equivalent to the broad language used for the distributively storing unit.

Examiner's Response regarding claims 2, 4, 7, 10, 12, and 15

Examiner submits that *Skodras et al.* does not fail to disclose a distributively storing unit as argued above. Given that the combination of the references teach or suggest all the limitations of claim 1, the rejections of claims 2, 4, 7-8, 10, 12, and 15-16 under 35 U.S.C. § 103 hold.

Drawings

[3] The drawings (fig. 3 and fig. 4) were received on June 27, 2008.

[4] The following is a quote from 37 C.F.R. § 1.84(q) (*emphasis added*):

> Lead lines are those lines between the reference characters and the details referred to. Such lines may be straight or curved and should be as short as possible. They must originate in the immediate proximity of the reference character and extend to the feature indicated. Lead lines must not cross each other. Lead lines are required for each reference character except for those which indicate the surface or cross section on which they are placed. Such a reference character must be underlined to make it clear that a lead line has not been left out by mistake. Lead lines must be executed in the same way as lines in the drawing.

[5] The drawings are objected to under 37 C.F.R. § 1.84(q) for failing to use lead lines (and when lead lines are not appropriate, replace with underlining) properly. For example, reference character 0LL in fig. 3 does not need a lead line, and should then be underlined.

[6] The following is a quote from 37 C.F.R. § 1.84(r):

> *Arrows* . Arrows may be used at the ends of lines, provided that their meaning is clear, as follows:
> (1) On a lead line, a freestanding arrow to indicate the entire section towards which it points;
> (2) On a lead line, an arrow touching a line to indicate the surface shown by the line looking along the direction of the arrow; or
> (3) To show the direction of movement.

[7] The drawings are objected to under 37 C.F.R. § 1.84(r) for failing to use arrows properly. For example, any arrows touching a surface should be a lead line (*e.g.*, reference character 80_{t1} should be a lead line).

[8] Corrected drawing sheets in compliance with 37 C.F.R. § 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 C.F.R. § 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 U.S.C. § 102

[9] The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

[10] **Claims 1, 3, 5, 9, 11, 13,** and **17** are rejected under 35 U.S.C. § 102(b) as being anticipated by The JPEG 2000 Still Image Compression Standard, IEEE Signal Processing Magazine, Sept 2001, p. 36-58 (*hereinafter* "Skodras et al.").

Regarding **claim 1**, *Skodras et al.* teaches an image processing apparatus ("computer" in left column, p. 38; fig. 2, p. 38) for hierarchically compressing ("Compressed Image Data" in fig. 2, p. 38) and coding ("Entropy Encoding" in fig. 2, p. 38) image data by subjecting pixel values of the image data ("Source Image Data" in fig. 2, p. 38) to a discrete wavelet transform ("Forward Transform" in fig. 2, p. 38; "[p]rior to computation of the forward discrete wavelet transform (DWT)…", left column, p. 40), quantization and coding for each of one or a plurality of rectangular regions into which the image data is divided ("The image components are (optionally) decomposed into rectangular tiles.", left column, p. 39; Image Tiling Section, right column, p. 39), the image processing comprising:

a hierarchical coding unit (unit responsible for producing the packet stream in fig. 11 in p. 45) to compress and code the image data in a state where the image data is divided for each hierarchical region (fig. 11, p. 45; "DWT on Each Tile" in fig. 3, p. 39 wherein the hierarchical regions are the image component itself (level -1), tiles (level 0), precinct (level 1), and code blocks (level 2)), to obtain compressed codes ("Code Stream" in fig. 11, p. 45), wherein the hierarchical coding unit comprises:

a first-level coding unit (coding unit responsible for coding all of the hierarchy levels in fig. 11) to receive the image data ("Image Component" and "Code Stream" in fig. 11) and to create the compressed codes of a first hierarchical layer (tiles (level 0) in fig. 11); and

a second-level coding unit (coding unit responsible for coding all of the hierarchy levels in fig. 11, whether or not it is the same or a different coding unit to the first coding unit) to receive a sub-band (the sub-band of the tile "layer" creates the whole precinct ("packet") as shown in fig. 11 by dashed lines on the right side) of the first hierarchical layer from the first-level coding unit and to create the compressed codes of a second hierarchical layer (precinct (level 1) in fig. 11), wherein the second hierarchical layer is a lower hierarchical layer than the first hierarchical layer (the precincts are at a lower hierarchical layer than tiles in fig. 11); and

a distributively storing unit ("Store and Transmit" in fig. 2, p. 38) to distributively store (fig. 11, p. 45 wherein each tile layer is a separate portion in the code stream) the compressed codes which are divided for each hierarchical layer by the hierarchical coding unit into a storage unit (it is implicit if not already inherent that the image processing apparatus computer of *Skodras et al.* has a memory storage unit), wherein the distributively storing unit comprises:

a first-level storing unit (those memory addresses responsible for storing the first hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) to store the compressed codes of the first hierarchical layer (tiles (level 0) in fig. 11); and

a second-level storing unit (those memory addresses responsible for storing the second hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) to separately store the compressed codes of the second hierarchical

layer (precinct (level 1) in fig. 11) from the compressed codes of the first hierarchical layer (tiles (level 0) in fig. 11), wherein the second-level storing unit (those memory addresses responsible for storing the second hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) is physically separate (addresses in the memory storing the first hierarchical layer are "physically separate" from the addresses in the memory storing the second hierarchical layer) from the first-level storing unit (those memory addresses responsible for storing the first hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses).

The same argument can be applied for the first hierarchical layer being the precinct layer and the second hierarchical layer being the code block layer as shown in fig. 11, OR from tile to code block, image component to tile, image component to precinct, OR image component to code block.

Regarding **claim 3**, claim 1 recites identical features as in claim 3. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 3. The means-plus-function language is anticipated by the computer hardware ("computer" in left column, p. 38; fig. 2, p. 38) of *Skodras et al.*

Regarding **claim 5**, *Skodras et al.* teaches an image processing apparatus ("computer" in left column, p. 38; fig. 2, p. 38) for hierarchically compressing ("Compressed Image Data" in fig. 2, p. 38) and coding ("Entropy Encoding" in fig. 2, p. 38) image data by subjecting pixel values of the image data ("Source Image Data" in fig. 2, p. 38) to a discrete wavelet transform ("Forward Transform" in fig. 2, p. 38; "[p]rior to computation of the forward discrete wavelet transform (DWT)…", left column, p. 40), quantization and coding for each of one or a plurality

of rectangular regions into which the image data is divided ("The image components are (optionally) decomposed into rectangular tiles.", left column, p. 39; Image Tiling Section, right column, p. 39), the image processing comprising:

a rectangular region coding unit ("Tiling" in fig. 3, p. 39) to compress and code the image data in a state where the image data is divided for each rectangular region ("DWT on Each Tile" in fig. 3, p. 39; "All operations, including component mixing, wavelet transform, quantization and entropy coding are performed independently on the image tiles (fig. 3).", right column, p. 39), to obtain compressed codes, wherein the rectangular region coding unit creates compressed codes for a first rectangular (tiles (level 0) in fig. 11; a rectangular region as evident in fig. 9 and fig. 3) and creates compressed codes for a second rectangular region (precinct (level 1) in fig. 11; a rectangular region as evident in fig. 9 ad fig. 3); and

a distributively storing unit ("Store and Transmit" in fig. 2, p. 38) to distributively store (fig. 11, p. 45 wherein each tile layer is a separate portion in the code stream) the compressed codes which are divided for each rectangular region by the rectangular region coding unit, wherein the distributively storing unit comprises:

a first storing unit (those memory addresses responsible for storing the first hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) to store the compressed codes of the first rectangular region; and

a second storing unit (those memory addresses responsible for storing the second hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) to separately store the compressed codes of the second rectangular region (precinct (level 1) in fig. 11; a rectangular region as evident in fig. 9 ad fig. 3) from the

compressed codes of the first rectangular region (tiles (level 0) in fig. 11; a rectangular region as evident in fig. 9 and fig. 3), wherein the second storing unit (those memory addresses responsible for storing the second hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) is separate (addresses in the memory storing the first hierarchical layer are "physically separate" from the addresses in the memory storing the second hierarchical layer) from the first storing unit (those memory addresses responsible for storing the first hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses).

Regarding **claim 9**, claim 5 recites identical features as in claim 9. Thus, references/arguments equivalent to those presented above for claim 5 are equally applicable to claim 9. The means-plus-function language is anticipated by the computer hardware ("computer" in left column, p. 38; fig. 2, p. 38) of *Skodras et al.*.

Regarding **claim 11**, claim 1 recites identical features as in claim 11. Thus, references/arguments equivalent to those presented above for claim 1 are equally applicable to claim 11.

Regarding **claim 13**, claim 5 recites identical features as in claim 13. Thus, references/arguments equivalent to those presented above for claim 5 are equally applicable to claim 13.

Regarding **claim 17**, *Skodras et al.* teaches an image processing apparatus ("computer" in left column, p. 38; fig. 2, p. 38) for hierarchically compressing ("Compressed Image Data" in fig. 2, p. 38) and coding ("Entropy Encoding" in fig. 2, p. 38) for each one or a plurality of rectangular regions ("DWT on Each Tile" in fig. 3, p. 39; "All operations, including component

mixing, wavelet transform, quantization and entropy coding are performed independently on the image tiles (Fig. 3).", right column, p. 39) into which the image data by subjecting pixel values of the image data ("Source Image Data" in fig. 2, p. 38) to a discrete wavelet transform ("Forward Transform" in fig. 2, p. 38; "[p]rior to computation of the forward discrete wavelet transform (DWT)…", left column, p. 40), quantization and coding for each of one or a plurality of rectangular regions into which the image data is divided ("The image components are (optionally) decomposed into rectangular tiles.", left column, p. 39; Image Tiling Section, right column, p. 39), the image processing comprising:

a hierarchical coding unit (unit responsible for producing the packet stream in fig. 11 in p. 45) to compress and code the image data in a state where the image data is divided for each hierarchical region (fig. 11, p. 45; "DWT on Each Tile" in fig. 3, p. 39 wherein the hierarchical regions are the image component itself (level -1), tiles (level 0), precinct (level 1), and code blocks (level 2)), to obtain compressed codes ("Code Stream" in fig. 11, p. 45), wherein the hierarchical coding unit comprises:

a first-level coding unit (coding unit responsible for coding all of the hierarchy levels in fig. 11) to receive the image data ("Image Component" and "Code Stream" in fig. 11) and to create the compressed codes of a first hierarchical layer (tiles (level 0) in fig. 11); and

a second-level coding unit (coding unit responsible for coding all of the hierarchy levels in fig. 11, whether or not it is the same or a different coding unit to the first coding unit) to receive a sub-band (the sub-band of the tile "layer" creates the whole precinct ("packet") as shown in fig. 11 by dashed lines on the right side) of the first hierarchical layer from the first-level coding unit and to create the compressed codes of a second hierarchical layer (precinct

(level 1) in fig. 11), wherein the second hierarchical layer is a lower hierarchical layer than the first hierarchical layer (the precincts are at a lower hierarchical layer than tiles in fig. 11); and

a distributively storing unit ("Store and Transmit" in fig. 2, p. 38) to distributively store (fig. 11, p. 45 wherein each tile layer is a separate portion in the code stream) the compressed codes which are divided for each hierarchical layer by the hierarchical coding unit into a storage unit (it is implicit if not already inherent that the image processing apparatus computer of *Skodras et al.* has a memory storage unit), wherein the distributively storing unit comprises:

a first-level storing unit (those memory addresses responsible for storing the first hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) to only receive the compressed codes (those memory addresses responsible for storing the first hierarchical layer only receive those codes to store) of the first hierarchical layer (tiles (level 0) in fig. 11) from the first-level coding unit (tiles (level 0) in fig. 11) and to store the compressed codes of the first hierarchical layer (tiles (level 0) in fig. 11); and

a second-level storing unit (those memory addresses responsible for storing the second hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) to only receive the compressed codes (those memory addresses responsible for storing the first hierarchical layer only receive those codes to store) of the second hierarchical layer (precinct (level 1) in fig. 11) from the compressed codes of the first hierarchical layer (tiles (level 0) in fig. 11), wherein the second-level storing unit (those memory addresses responsible for storing the second hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses) is physically separate (addresses in the memory storing the first hierarchical layer are "physically separate" from the

addresses in the memory storing the second hierarchical layer) from the first-level storing unit (those memory addresses responsible for storing the first hierarchical layer in the "[c]ode [s]tream" in fig. 11, and thus all hierarchical layers contained in those memory addresses).

The same argument can be applied for the first hierarchical layer being the precinct layer and the second hierarchical layer being the code block layer as shown in fig. 11, OR from tile to code block, image component to tile, image component to precinct, OR image component to code block.

Claim Rejections - 35 U.S.C. § 103

[11] The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

[12] **Claims 2, 4, 7, 10, 12,** and **15** are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Skodras et al.* in view of U.S. Patent No. 6,070,167 (issued May 30, 2000, *hereinafter* "Qian et al.").

Regarding **claim 2**, while *Skodras et al.* teaches an image processing apparatus ("computer" in left column, p. 38; fig. 2, p. 38) for hierarchically compressing ("Compressed Image Data" in fig. 2, p. 38) and coding ("Entropy Encoding" in fig. 2, p. 38) image data by subjecting pixel values of the image data ("Source Image Data" in fig. 2, p. 38) to a discrete wavelet transform ("Forward Transform" in fig. 2, p. 38; "[p]rior to computation of the forward discrete wavelet transform (DWT)…", left column, p. 40), quantization and coding for each of one or a plurality of rectangular regions into which the image data is divided ("The image

components are (optionally) decomposed into rectangular tiles.", left column, p. 39; Image Tiling Section, right column, p. 39), the image processing apparatus forming an electronic equipment (the computer to execute fig. 2, p. 38 forms electronic equipment) and comprising:

a hierarchical coding unit (unit responsible for producing the packet stream in fig. 11 in p. 45) to compress and code the image data in a state where the image data is divided for each hierarchical region (fig. 11, p. 45; "DWT on Each Tile" in fig. 3, p. 39 wherein the hierarchical regions are the tiles (level 0), precinct (level 1), and code blocks (level 2)), to obtain compressed codes ("Code Stream" in fig. 11, p. 45); and

a distributively storing unit ("Store and Transmit" in fig. 2, p. 38) to distributively store (fig. 11, p. 45 wherein each tile layer is a separate portion in the code stream) the compressed codes for each hierarchical layer separately by hierarchical layer (each hierarchical layer is stored in the addresses of memory, each address being physically separate from each other, *see* Claim 1 argument) into a storage unit (it is implicit if not already inherent that the image processing apparatus computer of *Skodras et al.* has a memory storage unit), *Skodras et al.* does not teach

(i) electronic equipment which is coupled to a network having other electronic equipments coupled thereto; and

(ii) distributively storing information into a storage unit of each of the other electronic equipments.

Qian et al. discloses a hierarchical method and system for object-based audiovisual descriptive tagging of images for information retrieval, editing, and manipulation (fig. 1) that teaches

(i) electronic equipment ("computer" in 2:58-67; fig. 1, items 12, 14, 15, 16, 17, 20) which is coupled to a network (fig. 1, item 18) having other electronic equipments coupled thereto (a computer network is by definition composed of multiple computers being connected together using a telecommunication system for the purpose of sharing data, resources, and communication); and

(ii) distributively storing information into a storage unit of each of the other electronic equipments (3:31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the electronic equipment of *Skodras et al.* to include having other electronic equipments coupled thereto as taught by *Qian et al.* and the distributively storing unit of *Skodras et al.* to include storing the hierarchical layered compressed codes as taught by *Qian et al.* "…to develop a hierarchical data structure and method that enables association of descriptive data in an image.", *Qian et al.*, 1:59-61 and "to provide a system and method where the descriptive data may be specific to objects in the image and may include textual information, links to other files, other objects within the same image or other images, or links to web pages, and object features, such as shape, and audio annotation.", *Qian et al.*, 1:62-67.

Regarding **claim 4**, claim 2 recites identical features as in claim 4. Thus, references/arguments equivalent to those presented above for claim 2 are equally applicable to claim 4. The means-plus-function language is anticipated by the computer hardware ("computer" in left column, p. 38; fig. 2, p. 38) of *Skodras et al.*.

Regarding **claim 7**, while *Skodras et al.* teaches an image processing apparatus ("computer" in left column, p. 38; fig. 2, p. 38) for hierarchically compressing ("Compressed

Image Data" in fig. 2, p. 38) and coding ("Entropy Encoding" in fig. 2, p. 38) image data by subjecting pixel values of the image data ("Source Image Data" in fig. 2, p. 38) to a discrete wavelet transform ("Forward Transform" in fig. 2, p. 38; "[p]rior to computation of the forward discrete wavelet transform (DWT)…", left column, p. 40), quantization and coding for each of one or a plurality of rectangular regions into which the image data is divided ("The image components are (optionally) decomposed into rectangular tiles.", left column, p. 39; Image Tiling Section, right column, p. 39), the image processing apparatus forming an electronic equipment (the computer to execute fig. 2, p. 38 forms electronic equipment) and comprising:

a rectangular region coding unit ("Tiling" in fig. 3, p. 39) to compress and code the image data in a state where the image data is divided for each rectangular region ("DWT on Each Tile" in fig. 3, p. 39; "All operations, including component mixing, wavelet transform, quantization and entropy coding are performed independently on the image tiles (Fig. 3).", right column, p. 39), to obtain compressed codes ("Code Stream" in fig. 11, p. 45); and

a distributively storing unit ("Store and Transmit" in fig. 2, p. 38) to distributively store (fig. 11, p. 45 wherein each tile layer is a separate portion in the code stream) the compressed codes for each rectangular region separately by rectangular region (each hierarchical layer is stored in the addresses of memory, each address being physically separate from each other, *see* Claim 1 argument) into a storage unit (it is implicit if not already inherent that the image processing apparatus computer of *Skodras et al.* has a memory storage unit), *Skodras et al.* does not teach

(i) electronic equipment which is coupled to a network having other electronic equipments coupled thereto; and

(ii) distributively storing information into a storage unit of each of the other electronic equipments.

Qian et al. et al. discloses a hierarchical method and system for object-based audiovisual descriptive tagging of images for information retrieval, editing, and manipulation (fig. 1) that teaches

(i) electronic equipment ("computer" in 2:58-67; fig. 1, items 12, 14, 15, 16, 17, 20) which is coupled to a network (fig. 1, item 18) having other electronic equipments coupled thereto (a computer network is by definition composed of multiple computers being connected together using a telecommunication system for the purpose of sharing data, resources, and communication); and

(ii) distributively storing information into a storage unit of each of the other electronic equipments (3:31-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the electronic equipment of *Skodras et al.* to include having other electronic equipments coupled thereto as taught by *Qian et al.* and the distributively storing unit of *Skodras et al.* to include storing the hierarchical layered compressed codes as taught by *Qian et al.* "…to develop a hierarchical data structure and method that enables association of descriptive data in an image.", *Qian et al.*, 1:59-61 and "to provide a system and method where the descriptive data may be specific to objects in the image and may include textual information, links to other files, other objects within the same image or other images, or links to web pages, and object features, such as shape, and audio annotation.", *Qian et al.*, 1:62-67.

Regarding **claim 10**, claim 7 recites identical features as in claim 10. Thus, references/arguments equivalent to those presented above for claim 7 are equally applicable to claim 10. The means-plus-function language is anticipated by the computer hardware ("computer" in left column, p. 38; fig. 2, p. 38) of *Skodras et al.*.

Regarding **claim 12**, claim 2 recites identical features as in claim 12. Thus, references/arguments equivalent to those presented above for claim 2 are equally applicable to claim 12.

Regarding **claim 15**, claim 7 recites identical features as in claim 15. Thus, references/arguments equivalent to those presented above for claim 7 are equally applicable to claim 15.

[13] **Claims 6** and **14** are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Skodras et al.* in view of U.S. Pub. No. 2002/0091665 (filed Jun. 15, 2001, *hereinafter* "Beek et al.").

Regarding **claim 6**, while *Skodras et al.* discloses the image processing apparatus as claimed in claim 5, though *Skodras et al.* hints at other forms of decomposition (besides tiles) citing "The image components are (optionally) decomposed into rectangular tiles. The tile-component is the basic unit of the original or reconstructed image.", left column, p. 39), *Skodras et al.* does not teach wherein the rectangular region coding unit compresses and codes the image data with a decomposition level dependent on a type of the image data, a type of region of the image data, a type of source electronic equipment of the image data, or an external instruction.

Beek et al. discloses metadata in JPEG 2000 file format that teaches "external instruction" with use of the functions SegmentDecomposition Decomposition, DecompositionDataType Datatype and DecompositionType Attribute (¶¶ 0036-0038).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for rectangular region coding unit as taught by *Skodras et al.* to compress and code the image data with a decomposition level dependent on external instruction as taught by *Beek et al.* "…so that all complaint JPEG2000 viewers will be able to render the image in a proper manner and in addition process the additional information, if desired.", *Beek et al.*, ¶ 0016.

Regarding **claim 14**, claim 6 recites identical features as in claim 14. Thus, references/arguments equivalent to those presented above for claim 6 are equally applicable to claim 14.

[14] **Claims 8** and **16** are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Skodras et al.* in view of *Qian et al.* and *Beek et al.*

Regarding **claim 8**, claim 6 recites identical features as in claim 8. Thus, references/arguments equivalent to those presented above for claim 6 are equally applicable to claim 8.

Regarding **claim 16**, claim 6 recites identical features as in claim 16. Thus, references/arguments equivalent to those presented above for claim 6 are equally applicable to claim 16.

Conclusion

[15] Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID P. RASHID whose telephone number is (571)270-1578. The examiner can normally be reached Monday - Friday 7:30 - 17:00 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on (571) 272-74155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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